REMARKS

These remarks are responsive to the Office Action mailed July 7, 2008 ("Office Action").

STATUS OF THE CLAIMS

Claims 1-24 are currently pending in the present application, with claims 1, 10, and 24 being the independent claims. Claims 1, 2, 9, 10, 14, and 20-24 are currently amended.

35 USC § 103(a)

The Office Action rejects claims 1-24 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Pat. No. 6,515,826 to Hsiao et al. (Hsiao) in view U.S. Pat. No. 6,242,320 to So (So), and further in view of Hartmannsgruber, et al., "A Selective CMP Process for Stacked low-k'CVD Oxide Films", Microelectronic Engineering, Vol. 50, pg. 53-58, 2000 (Hartmannsgruber).

Paragraph 13 of the Office Action states the following:

> *Also, as for the limitation of "said active wafer provided for receiving an active circuit in a later step" (claim 1) recitation of the claimed invention does not result in a structural difference between the claimed invention and the prior art, thus claimed invention is only an art recognized suitability for an intended purpose, MPEP 2144.07.*

Paragraph 16 similarly recites the following:

> *Finally, a recitation of "said first wafer for receiving an active circuit in a later stage" and "for monitoring the reduction in thickness of the claimed invention does not result in a structural difference between the claimed invention and the prior art, thus claimed invention is only an art recognized suitability for an intended purpose, MPEP 2144.07.*

Applicant respectfully requests clarification on how the alleged lack of a structural difference between the claimed invention and the prior art -- and, indeed, MPEP § 2144.07 as a whole -- are in any way relevant to the patentability of claim 1.

Further, Applicant respectfully emphasizes that claim 1 recites **a method** of manufacturing. The method needs method steps to distinguish. The method steps may

work or operate structure, but they do not necessarily need structure to distinguish. The Examiner's attention is respectfully directed to the last feature recited in claim 1, where the active circuit **is formed** in the active wafer. The active wafer is one of the two wafers that form the bonded pair of wafers (see lines 1 to 3 of claim 1 and the final paragraph of claim 1). Applicant respectfully submits that the claimed invention recites a a distinguishing method step.

Further, Applicant respectfully submits that the claimed feature of *optically detecting said exposure of the reference trench* is an additional recitation of the claimed method that is neither taught nor suggested by the combination of references cited in the Office Action. This is an optical step to detect the exposure of a trench that has substantially a depth that corresponds to the targeted thickness of the third group of features.

The Office Action's application of Hsiao:

Paragraph 4 of the Office Action provides a discussion of Hsiao as applied to various claim recitations

In general response to the application of Hsiao to the claimed invention, Applicant respectfully submits that in Hsiao column 6, line 36 to column 8, line 24 and figure 15 **no wafer pair** is shown that is bonded together. Figure 15 shows an aluminum layer 304, which is not a semiconductor wafer. This layer cannot be "removed", which would be needed when the top down representation of figure 15 is bonded onto another wafer, to allow optical detection of reduction of thickness, by removing wafer material from the aluminum layer 304 downwards. Optical detection would also fail, because the two broadest trenches 332, 336 have the same width and reach down to the aluminum layer 304. They provide the same depth. The claim requires **a systematic row** of trenches and a reference trench that is neighboured by a shallower and a deeper trench. Trenches 332, 336 in Hsiao have the same width and the same depth. They cannot be used as a precise monitoring structure.

Paragraph 4 of the Office Action points to Figure 15 of Hsiao as allegedly showing a test structure. Applicant respectfully disagrees. There is no test structure shown and described, there is shown a structure that explains and visualizes the dependency of the RIE lag phenomena, see column 7, line 29 to 35. The relationship between width and depth is shown. The test structure that is used for monitoring the

thickness reduction in our method claim 1 is not explained in Hsiao, and the word test structure is nowhere used in Hsiao.

Paragraph 4a of the Office Action alleges that Hsiao discloses the claimed recitation of "said wafer receiving an active circuit ... in a later stage." Applicant respectfully submits that this active circuit is provided in the active wafer in the last group of features of our claim 1. The Examiner cannot properly compare this to the two different types of putting electrical members into the opening 164, 168 of for example figure 10 or figure 11 in the corresponding trenches 172, 176 of different width. This is explained in column 5, line 40 to 44. The coil openings and the electrical interconnect opening are treated different and this is placed into the trenches. There is no active circuit in the active wafer as presently claimed. Rather, the claim describes **forming the active circuit** in the wafer. This is not shown in Hsiao.

Paragraph 4(b) of the Office Action suggests that active wafer 300 (not 2) receives a removal action or a removal step. Applicant respectfully submits that no such removal step is shown from the aluminum layer 304, which would correspond our figure 2 and the top surface 2b. When no removal action is there, the reference trench as assumed 350 about in the centre of the row of trenches in figure 15 of Hsiao cannot be exposed, and therefore not optically detected. The third full feature of our claim is not shown in Hsiao and is not suggested in Hsiao.

For at least these reasons, Applicant respectfully submits that Hsiao can not be properly applied to the claimed subject matter as presently alleged.

The "So" reference does not cure the acknowledged deficiencies of Hsiao:

Paragraph 5 of the Office Action acknowledges the deficiencies of Hsiao. Specifically the Office Action states that "Hsiao fails to teach the bonding of a carrier wafer after creating the trenches and the use of a polishing process on the backside of the active wafer made of silicon until exposing the reference trench."

Paragraph 6 of the Office Action introduces So into the rejection and alleges that So cures the acknowledged deficiencies of Hsiao. Specifically, the Office Action relies on column 2, line 66 -- column 4, line 51 in conjunction with Figure 2G.

The bonding of carrier wafer is not shown. In fact, paragraph 5 of the Office Action has several deficiencies that have previously been identified in paragraph 4 of the action **to belong** to the teaching of Hsiao. The bonding is not shown in Hsiao. The active wafer is not bonded to a base wafer. This was addressed above. The use of a

removal process from the backside is claimed in claim 1. It is termed to be a removal process. Hsiao does not remove anything through the aluminum layer 304 and it is said in 4b of the Office Action that a removal is there. In paragraph 5 the Examiner says that no polishing process from the backside (i.e. is the removal process from the backside of the active wafer) is present in Hsiao. The Examiner reverses his arguments between paragraphs 4 and 5. The exposing of the reference trench in paragraph 5 is also not shown in Hsiao, to the contrary in paragraph 4b is said that removal leads to an exposure of the reference trench 350, which is understood to be "to correspond to a depth of this reference trench 350". Paragraph 5 says this is not present in Hsiao, paragraph 4b says it is present. There are several deficiencies in paragraph 5 that the Examiner seeks to find in So.

Further, Paragraph 6 of the Office Action alleges that the plurality of different trenches has different depths 23, 24 in So. Figures 2A to 2I show **only two depths of trenches.** One is used as a first polishing stopper, column 4, line 12. This is the higher (deeper) trench and the isolation layer 25 that is contained in this trench. Our claim teaches a systematic row of trenches and the systematic row is explained by the reference trench, at least, that is neighboured by a shallower and a deeper trench. Not figure 2G and none of the other figures of So does disclose this relation of a systematic row. The second trench depth 23 also filled with an isolation layer is also a polishing stopper, column 4, line 30. Two polishing steps are stopped at two trench depths. The result is shown in figure 2I. Here we cannot find a monitoring of thickness reduction using the systematic row of trenches and the certain definite depths that are claimed in claim 1 and not just said to be "different depths".

Further, paragraph 6d alleges that So teaches that removing is done from the backside of the active wafer. Applicant agrees that this removing is done from the backside, but the removing stops at the two specified depths of the two different types of trenches that are filled with isolation layer, 23, 25. The removal process we claim ends at the targeted thickness after the end of the removing of material and is stopped when hitting the reference trench that has a neighboured other trench that is deeper and another neighboured trench that is shallower. Paragraph 6d of the Office Action does not expose a reference trench as identified in our claim. It exposes the filling of a reference trench at the end of a polishing process, but not identifying another trench left and another trench right to this, one being already exposed and the other one not yet being exposed. This is then optically detected in the fourth feature of presently recited claim 1.

Paragraph 7 of the Office Action alleges that So provides evidence that a person of ordinary skill in the art would find a reason, suggestion, or motivation to combine the double wafer structure of So into the device of figure 15 of Hsiao. Applicant respectfully disagrees. Hsiao cannot be removed or polished from the aluminum side 304. There is no motivation to combine matters that cannot function together. And still, no test structure is shown in Hsiao and also not shown in So, so a further feature of "optically detecting the exposure of the reference trench for monitoring the thickness reduction" is not contained in both documents.

Paragraph 8 of the Office Action includes similar assertions to those presented in paragraph 7. For reasons discussed above, Applicant respectfully disagrees with the Office Action's conclusion that it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Hsiao and So. So has no reference trench that is exposed, instead trenches are filled with isolating material, 23, 25, see column 4, line 10/12 and 33/34. The aim to have a "uniform semiconductor layer" as taught in So, column 4, line 35 to 37, is not found in Hsiao. Hsiao does not remove material and has a bar as aluminum layer 304. Nothing is fairly suggested to be combined, apart from hindsight combination of isolated features in prior art. Item 8 of the Office Action does not have convincing character.

Hartmanngruber fails to cure the acknowledge deficiencies of Hsiao and So:

Paragraph 9 of the Office Action acknowledges that neither Hsiao or So, when taken alone or in combination, disclose the use of an optical device in the claimed method.

The Office Action introduces Hartmanngruber to cure this acknowledged deficiency. Applicant respectfully submits that Hartmannsgruber does not fairly suggest using an optical detector; instead, Hartmannsgruber suggests to use a profilometer, which is not at all an optical device. It is a surface testing device by mechanical contact. This device is not useful for either document So or Hsiao. For So the trenches are filled and cannot be tested by a mechanical device. The exposed trenches 23, 25 in figure 2I have no surface difference with respect to the remaining active layer 21a, and the device of Hartmannsgruber would be useless when taken into So. It would also be useless when taken into figure 15 of Hsiao as nothing can be tested there, the aluminum layer 304 is still solid and flat, and the other openings 312 just define the ratio according to figure 16

of width to depth of the trenches, not being used for detection of a certain removal depth of the wafer from the backside as claimed in claim 1.

Independent Claims 10 and 24 are allowable over the cited references:

Claim 10 is allowable for the reasons given above. The device for monitoring contains the test structure and has the systematic row, having at least the reference trench in it. The "different width in a defined manner" suggests that there are different depths of the trenches, as given in figure 16 of Hsiao, where the relation of depth and width is shown. The removal process in claim 10 exposes the reference trench. It exposes the bottom end of the reference trench by removing the bottom, which actually makes the reference trench exposed. This is done in the systematic row of a plurality of trenches, each one having a different width, now is clarified in the claim 10, first feature, as the previous reading could be differently interpreted, what actually was not done by the Examiner.

The structure claim 10 has the active circuit in the first wafer as a structural feature, see first characterizing portion. This is not an intention and it is not a suitability, items 13 and 16 of the Examiner's action. This is a structural difference against at least Hsiao. So does not fairly suggest to use a reference trench according to the third feature to define the target thickness of the removal process. The bottom of the trench is also not exposed in So as those trenches are filled with insulation material. Only the insulation material can be exposed, but not the empty trench that has nothing in it, see claim 11 for the device and claim 4 for the method of claim 1.

The same applies to claim 24. This method claim has several steps and the exposure of the reference trench is the monitoring of the thickness reduction. We have termed the wafers here to be active and carrier wafer. We are also doing the reduction monitoring during the production. This is new in the claim and in the final feature we say that several neighbouring trenches on one side of the reference trench and several other neighbouring trenches on the other side have certain depths. One are deeper and the other ones are shallower. This gives the reference trench a certain meaning. This claim is allowable for reasons given for claim 1.

CONCLUSION

Pursuant to 37 CFR § 1.136(a), Applicant hereby petitions for a One-Month Extension of Time. Commissioner is hereby authorized to charge fees in the amount of $130.00 as set forth under 37 CFR § 1.136(a) for the One-Month Extension of Time, to include responding up through November 10, 2008. In the event any variance exist, the Commissioner is hereby authorized to debit or credit undersigned's Deposit Account No. 50-0206 to cure any such underpayments or overpayments of fees as required.

A notice of allowance is earnestly solicited.

Respectfully submitted,

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